HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P. O. Box 272400
Fort Collins, Colorado 80527-2400

Image

AF/2823

PATENT APPLICATION

ATTORNEY DOCKET NO. 10002861 -1

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Zhizhang Chen et al

Confirmation No.: 9286

Application No.: 09/817703

Examiner: George Fourson

Filing Date: Mar 26, 2001

Group Art Unit: 2823

Title: LDMOS And CMOS Integrated Circuit And Method Of Making

Mail Stop Appeal Brief-Patents
Commissioner For Patents
PO Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF APPEAL BRIEF

Sir:

Transmitted herewith in **triplicate** is the Appeal Brief in this application with respect to the Notice of Appeal filed on **Feb 18, 2004**.

The fee for filing this Appeal Brief is (37 CFR 1.17(c)) $330.00.

(complete (a) or (b) as applicable)

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136(a) apply.

( ) (a) Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d) for the total number of months checked below:

( )	one month	$110.00
( )	two months	$420.00
( )	three months	$950.00
( )	four months	$1480.00

( ) The extension fee has already been filled in this application.

(X) (b) Applicant believes that no extension of time is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

Please charge to Deposit Account **08-2025** the sum of **$330.00**. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that may regulate fees. A duplicate copy of this sheet is enclosed.

(X) I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, Alexandria, VA 22313-1450. Date of Deposit: 3/19/04

OR

( ) I hereby certify that this paper is being transmitted to the Patent and Trademark Office facsimile number_____ on _____

Number of pages:

Typed Name: Timothy F. Myers

Signature: Timothy F Myers

Respectfully submitted,

Zhizhang Chen et al

By Timothy F Myers

Timothy F. Myers

Attorney/Agent for Applicant(s)

Reg. No. **42,919**

Date: 3/19/04

Telephone No.: **541 715 4197**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re application of: Z. Chen et al. Art Unit: 2823
Examiner: George Fourson III

Serial Number: 09/817,703
Filed: March 26, 2001
Title: LDMOS AND CMOS INTEGRATED CIRCUIT AND METHOD OF MAKING
Date: March 19, 2004

APPEAL BRIEF UNDER 37 CFR §1.192

TO THE ASSISTANT COMMISSIONER FOR PATENTS:

Sir:

This Brief is submitted in triplicate in support of the Appeal in the above-identified application.

1. REAL PARTY IN INTEREST

The real party of interest is Hewlett-Packard Company. The assignee is Hewlett-Packard Development Company, LP, a Texas limited partnership and a wholly owned affiliate of Hewlett-Packard Company.

2. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

3. STATUS OF THE CLAIMS

Claims 10, 12, 14 and 16 are pending in the application. Claims 10 and 16 are allowed. Claims 12 and 14 stand finally rejected by the Examiner as noted in the Final Action dated January 23, 2004. Claims 12 and 14 are the subject of this Appeal.

4. STATUS OF AMENDMENTS

There have been no amendments filed subsequent to the final rejection.

5. SUMMARY OF THE INVENTION

The present invention is directed to a process for providing both high-voltage 30 and low-voltage transistor devices 26, 28 in a common substrate 10 (see Figs. 1 and 2) that eliminates several process steps used in conventional processes. The invention simplifies and reduces the cost of conventional processes by redesigning the Well dopant concentrations and foregoing the V_t adjust implant process steps (see Figs. 3A and 3B) while maintaining substantially the same threshold voltages and breakdown voltages of the conventional processes. Thus, well doping alone is used to control the V_t of the NMOS and PMOS low-voltage transistors (26, 28). For example, in one embodiment P-Well doping is used to control NMOS V_{tn} and N-Well doping is used to control PMOS V_{tp}, separately, without using the V_t adjust implant. This simplified process (see Figs. 5A-5I) not only eliminates the V_t implant step (Fig. 5K) but also allows use of a single N-Well dopant concentration for both low-voltage PMOS and high-voltage LDMOS transistors. The improved process eliminates at least two photo mask layers (one N-Well mask and the V_t block mask), two implants (one N-Well implant and the V_t adjust implant) and one furnace operation (channel oxidation prior to the V_t implant). Significant process cost reduction and cycle time is achieved. The changes in process flow between conventional and new processes occurs during the early stage of the new process, thus allowing the remaining steps of the new process to remain the same as with the conventional process.

6. ISSUE(S)

- Did the Examiner properly establish a case of *prima facie* obviousness, as required by *In re Lintner*[1], in rejecting claims 12 and 14 under 35 USC §103(a) over Tada in combination with Contiero et al.?

7. GROUPING OF THE CLAIMS

Applicants expressly state that the rejected claims do not rise or fall together as a single group. Applicants consider the following groups of claims to be separately patentable for the reasons stated below in the Argument section:

Group	*Claims in Group*
I	Claims 12 and 14

8. ARGUMENT

8A. Overview

Applicants are under no illusion that their invention is going to end up in the inventors hall of fame. Instead, Applicants' invention as claimed covers a relatively simple but elegant concept: a process for forming both high voltage and low voltage transistors on a substrate with a minimal amount of process steps such that a first conductivity type low voltage transistor and a second conductivity type low voltage transistor are created without a conventional threshold (V_t) implant step. To do so, during the process, a doping step is performed that both controls the threshold voltage of the second conductivity type low voltage transistor and sets the breakdown voltage of a first conductivity type high voltage transistor. Another doping step is used to control the threshold voltage of the first conductivity type low voltage transistor. It is Applicants' belief that the Examiner

[1] *In re Lintner*, 458 F.2d 1013, 173 USPQ 560, 562 (CCPA 1972).

has failed to consider their invention as a whole. Rather than ascertaining whether or not the cited reference teaching would appear to be sufficient for one of ordinary skill in the art to make the combination, the Applicants believe the Examiner is incorrectly using Applicant's claimed invention as a template to combine the various elements found in the cited references.[2] Further, the Examiner must consider the prior art in its entirety, including those disclosures that teach away from the Applicants' claimed invention.

Accordingly, these errors by the Examiner have resulted in the failure of the Examiner's obligation to perform the duty of establishing a *prima facie* case of obviousness in making a rejection under 35 USC § 103.

8B. Did the Examiner properly establish a case of *prima facie* obviousness, as required by *In re Lintner*, in rejecting claims 12 and 14 under 35 USC §103(a) over Tada in combination with Contiero et al.?

On Page 2 of the Final Action and Section 7 of the Office Action dated 10/20/2003, the Examiner rejected claims 12 and 14 under 35 USC 103(a) as being unpatentable over Tada in combination with Contiero et al. Applicants respectfully traverse this rejection. It is improper to combine Tada with Contiero, as there is no objective reason to make this combination for the reasons stated below.

As stated in In re Lintner[3] a prima facie case of obviousness requires the PTO to "ascertain whether or not the reference teachings would appear to be sufficient for one of ordinary skill in the relevant art having the references before him to make the proposed substitution, combination or other modification." "To reach a proper conclusion under §103, the decision maker must step backward in time and into the shoes worn by that "person" when the invention was unknown and just before it was made. In light of all the evidence, the decision maker must then determine whether the . . . claimed invention as a whole would have been

[2] Id.
[3] Id.

obvious at that time to that person."[4] Further, "obviousness under 35 USC 103 ((1982) & Supp. III 1985) is a legal issue, the determination of which involves factual inquires into (1) the scope and content of the prior art, (2) the level of ordinary skill in the art, (3) the differences between the claimed invention and the prior art, and (4) any objective evidence of non obviousness, such as long felt need, commercial success, failures of others."[5] The Applicants believe the Examiner has failed to perform such a factual inquiry and has inappropriately used Applicants' claimed invention as a template to make the various 103 combinations.

For instance in regard for claim 12, Applicants are claiming "doping the first and second regions with a first dopant concentration *to both control the threshold voltage* of the second conductivity type low-voltage transistor and *set a breakdown voltage* of the first conductivity high-voltage transistor." Similarly for claim 14, Applicants are claiming "doping the first and second regions with a first dopant concentration thereby *determining a threshold voltage* of the second conductivity type low-voltage transistor *and a breakdown voltage* of the first conductivity type high-voltage transistor." Therefore, Applicants are using one doping step to perform two functions, 1) setting the threshold voltage of the 2nd conductivity LV transistor, and 2) setting the breakdown voltage of the 1st conductivity HV transistor. Neither Tada nor Contiero alone or in combination disclose, teach or suggest this limitation. The Examiner in the Final Office Action clarifies his justification for the motivation to combine Tada and Contiero by stating that while "Tada does disclose forming a high voltage transistor but not disclose forming one having the first conductivity type," "Contiero is relied upon as teaching the suitability of forming the high voltage transistor of Tada as having the first conductivity type." The Examiner then states that it would have been obvious ... to combine the teachings of Tada and Contiero to enable the high voltage transistor formation step of Tada to be performed according to the teaching of Contiero. . . . Applicants respectfully traverse this statement for several reasons.

First, one of ordinary skill simply would not be motivated to look to Contiero for a high voltage transistor having the first conductivity type because contrary to

[4] Panduit Corp. v. Dennison Manufacturing Co., 1 USPQ 2d 1593, 1595-96 (Fed. Cir.), cert. Denied, 481 U.S. 1052 (1987).

[5] Allen Archery Inc. v. Browning Manufacturing Co., 2 USPQ.2d 1490, 1493 (Fed. Cir. 1987).

what the Examiner states, Tada does disclose a high voltage transistor of the first conductivity type as transistor 103 in Fig.1. However, this first conductivity type high-voltage transistor 103 is not in the second region and thus doped at the same time as the first region as Applicants are claiming. Thus, Applicants' claimed limitation does not read on Tada. The Examiner is essentially asserting that even though one of ordinary skill has a high voltage transistor of the first conductivity type, one of ordinary skill would be motivated to get the type of first conductivity HV transistor from Contiero and drop it into the second region "because it would enable the high voltage transistor 103 of Tada to be formed" (page 4, 10/20/2003 Office Action). However, because Tada already has a high voltage transistor 103 but made in another region (by a different process), there is no reasonable motivation to look to Contiero to add another high voltage transistor of a first conductivity type for the second region unless Applicants' disclosure is used as the template to make the suggestion.

Second, the Examiner has not considered all that the references teach and instead has chosen to select individual components of the references without looking at all that is taught, including those limitations that teach away from Applicant's invention. "[P]rior art references before the tribunal must be read as a whole and consideration must be given where the references diverge and teach away from the claimed invention. . . . Moreover, [one] cannot pick and choose among individual parts of assorted prior art references "as a mosaic to recreate a facsimile of the claimed invention."[6] Combining the high voltage transistor of a first conductivity type from Contiero into the second region using the teachings of Tada would not create the Applicants' claimed process. Tada discloses (col. 8, lines 27-47) that the channel doping step ("the additional voltage threshold adjust step" in Applicants claim language) is not required because of how the method of forming the gate electrode structures is done in Tada. That is, "since both sides of the high voltage n channel type MOSFET 103 and the high voltage p channel type MOSFET 104, *the conducting types of the channel formation region and the gate electrodes are the same*, the variation in the threshold voltage derived form the difference of mutual work functions so that the control of the threshold voltage can be easily made [sic]. Additionally, the gate electrode 11b is a p type to

correspond to the high voltage p channel type MOSFET 104, so that the threshold voltage can be more easily controlled than in an n-type gate electrode" (such as the first conductivity type high voltage transistor of Contiero). Therefore, placing a first conductivity high voltage transistor in the second region would result in a gate electrode structure having a different doping than that of the channel formation region and thus the threshold voltage would not be as controllable. A channel doping step would need to be performed as the requirement to eliminate it as taught by Tada is destroyed by the combination. Thus, without the Applicants disclosure to teach how to form the first conductivity transistor in the second region without the additional voltage threshold adjustment step, there is no motivation to combine Tada with Contiero. Again, the Examiner is ignoring the teachings of the references and accordingly using the Applicants' disclosure as a template to make the combination.

Third, the Examiner has failed to look at Applicant's claimed invention as a whole but merely looked at what was different between the Applicant's claimed invention and the various cited references. "[A]lthough Graham v. John Deere Co., . . . requires that certain factual inquiries, among them the differences between the prior art and the claimed invention, be conducted to support a determination of the issue of obviousness, the actual determination of the issue requires an evaluation in light of the findings in those inquires of the obviousness of the claimed invention as a whole, not merely the differences between the claimed invention and the prior art."[7] The Applicants believe that the Examiner has failed to consider Applicants' invention and indeed the references 'as a whole.' As stated by the Federal Circuit, "the claimed invention must be considered as a whole, and the question is *whether there is something in the prior art as a whole* to suggest the desirability, and thus the obviousness, of making the combination."[8] For instance, the Examiner states that the Applicants argument regarding the use of the same thickness of gate oxide for both transistors is not well taken because the claims are not so limited (page 2 of the Final Action, lines 14-15). However, Applicant is not using the argument of "same thickness of gate

---

[6] Akzo N.V. v. United States International Trade Commission, 1 USPQ.2d 1241, 1246 (Fed. Cir 1986), cert. Denied, 482 U.S. 909 (1987).

[7] Lear Siegler; Inc. v. Aeroquip Corp., 221 USPQ 1025, 1033 (Fed. Cir. 1984).

oxide" as an aspect of novelty to show differences but to show rather that Tada *teaches away* from Applicants' claimed limitation of "doping the first and second regions with a first dopant concentration *to both control the threshold voltage* of the second conductivity type low-voltage transistor and *set a breakdown voltage* of the first conductivity high-voltage transistor." Tada does not dope the first and second regions with a first dopant concentration to control both the threshold voltage of the second conductivity type low-voltage transistor and set a breakdown voltage of the first conductivity high-voltage transistor. Rather, Tada uses gate oxides of a greater thickness to control breakdown voltage for the high voltage transistor (see col. 5, lines 45-56 and col. 9, lines 37-43), not "doping the first and second regions . . ." as Applicants are claiming . As noted earlier, Tada doesn't even have the first conductivity high-voltage transistor within the second region so the Examiner is simply asserting combining the one from Conceirto in the second region. However, unless the Applicants' disclosure is used to make substitution of using doping rather than channel oxide thickness to control the breakdown voltage of the high voltage transistor of the first conductivity type, there is no motivation in Tada to combine with Concierto. Again, this is another example of the Examiner not considering the teachings of the references for all that they disclose but rather using Applicants' disclosure as the template to make the combination.

In addition, Applicants believe the Examiner may be considering that the reduction of process steps by the Applicants in their claimed process results in a "far simpler" process and thus would seem obvious in hindsight. However, "it is to be noted that simplicity and hindsight are not proper criteria for resolving the issue of obviousness."[9] "Furthermore, it is well settled that where the claimed invention solves a problem, the discovery of the source of the problem and its solution are considered to be part of the "invention as a whole" under 35 USC 103."[10] One ongoing problem in a semiconductor manufacturing environment is the tradeoff between product cost and accordingly device reliability and yields. Usually as costs are decreased, reliability and yields suffer. Conversely, Applicants' claimed process has allowed for the creating of an IC that allows both high voltage and low

[8] Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co., 221 USPQ 481, 488 (Fed. Cir. 1984)

[9] Ex parte Clapp, 227 USPQ 972, 973 (B.P.A.I. 1985).

voltage transistors to be formed on a single substrate while eliminating several process steps used in conventional processes to create the devices, thus reducing cost and while yet improving reliability and yields. This is done by using well doping alone to control the threshold voltages of the NMOS and PMOS low-voltage transistors. Simply combining the first conductivity type high voltage transistor from Conceirto with Tada without modify all the process steps that are taught in Tada and Conceirto would not result in Applicant's claimed invention without the teachings of Applicants' disclosure. For instance, Contiero discloses numerous additional process steps such as needed for the formation of the n+ buried layers 3 and the p type bottom isolations 4 (see col3, lines 40-45 and Fig. 1). Thus, the Examiner has not considered Applicants' claimed invention as a whole when only evaluating Tada and Conceirto alone without the Applicants' disclosure as guidance.

"It should not be necessary . . . to point out that a patentable invention may lie in the discovery of the source of a problem even though the remedy may be obvious once the source of the problem is identified. This is part of the "subject matter as a whole" which should always be considered in determining the obviousness of an invention under 35 USC 103."[11] "Moreover, the conception of a new and useful improvement must be considered along with the actual means of achieving it in determining the presence or absence of invention. . . . The discovery of a problem calling for an improvement is often a very essential element in an invention correcting such a problem; and though the problem, once realized, may be solved by use of old and known elements, this does not necessarily negative invention."[12] "The court must be ever alert not to read obviousness into an invention on the basis of the applicant's own statements; that is, we must view the prior art without reading into that art appellant's teachings. . . . The issue, then, is whether the teachings of the prior art would, in and of themselves and without the benefits of appellant's disclosure, make the invention as a whole, obvious."[13] Applicants believe that without the Applicants' disclosure, a person of ordinary skill in the art at the time the invention was made would not

---

[10] Ex parte Hiyamizu, 10USPQ.2d 1393, 1394-95 (BPAI 1988).
[11] In re Nomiya, 184 USPQ 607, 612 (CCPA 1975).
[12] In re Bisley, 94 USPQ 80, 86-87 (CCPA 1952).
[13] In re Sponnoble, 160 USPQ 237, 243 (CCPA 1969).

have been able to deduce Applicants' claimed invention without the knowledge gleaned from Applicants' disclosure as discussed above.

In summary, the Applicants believe that the Examiner is not considering their claimed invention as a whole. As MPEP 2141.02 states, "in determining the differences between the prior art and the claims, the question under 35 USC 103 is not whether the differences themselves would have been obvious, but whether the claimed invention as a whole would have been obvious." It is not whether the different elements of the claim are known, but whether the claimed combination has been disclosed, taught or suggested in the art. The Examiner has not met this requirement. Again the MPEP in 2141.02 states that "although a prior art device 'may be capable of being modified to run the way the apparatus is claimed, there must be a suggestion or motivation in the reference to do so.'" The fact that the claimed invention is within the capabilities of one of ordinary skill in the art is not sufficient by itself to establish *prima facie* obviousness." It was improper for the Examiner to take the first conductivity type high voltage transistor from Concerto to add to Tada without examining that Tada already had a high voltage first conductivity type transistor and that further taught controlling the breakdown voltage by varying the gate oxide thicknesses. Further, Tada teaches having the gate material and the channel type be of the same conductivity to allow for the removal of the threshold adjustment step. Adding the first conductivity type of high voltage transistor from Concierto to the second region would violate this teaching of Tada and thus one of ordinary skill in the art would not be motivated to make the combination without the teachings of the Applicants' disclosure. Indeed, Applicant believes the Examiner is using the Applicants claimed invention as a template or guide to combine separate disclosures which do not disclose, teach, or suggest Applicant's claimed invention. Thus, the rejection under 35 USC 103(a) was improper. Withdrawal of the rejection under 35 USC 103(a) and allowance of claims 12 and 14 is respectfully requested.

9. Conclusion

The Examiner erred in failing to establish a case of *prima facie* obviousness in rejecting claims 12 and 14. Applicant respectfully requests reversal of these rejections from the Board of Patent Appeals and Interferences, along with timely issuance of a notice of allowance indicating that claims 10, 12, 14 and 16 are allowed.

Applicant will defer his decision as to whether or not to request oral argument until after receipt of the Examiner's Answer to this Appeal Brief.

Respectfully Submitted,

Z. Chen et al.

By: 

Timothy F. Myers
Patent Attorney
Registration No. 42,919

Hewlett-Packard Company
Legal Department
MS 422B
1000 NE Circle Blvd.
Corvallis, OR 97330
Telephone: (503)715-4197
Fax: (503)715-8581

APPENDIX

Claims

10. A method of creating a substrate having multiple regions for creating low-voltage transistors of a first and second conductivity and high-voltage transistors of a first conductivity, consisting essentially of the steps of:

creating a defined deposition of a first dielectric layer to expose a first region and a second region;

implanting a first conductivity dopant into the first and second regions;

applying a first protective coating over the first and second regions;

driving in the first conductivity dopant into the substrate;

removing the first dielectric layer;

creating a defined deposition of a second dielectric layer in the same location as the defined deposition of the first dielectric layer;

implanting a second conductivity dopant in the substrate disposed under the defined deposition of the second dielectric layer;

driving in the second conductivity dopant into the substrate;

removing the first protective coating and the second dielectric layer;

creating a patterned third dielectric layer over the surface of the substrate to expose the drain and source of the first and second conductivity low-voltage transistors and the first conductivity high-voltage transistor;

creating a defined deposition of a fourth dielectric layer disposed on the drain and source of the first conductivity low-voltage transistor;

applying a second protective coating over the first and second regions;

implanting a second conductivity dopant into the substrate disposed under the drain and source of the first conductivity low-voltage transistor;

removing the second protective coating;

creating a fifth dielectric layer in areas of the substrate where the third dielectric layer is not located;

removing the patterned third dielectric layer; and

then further comprising the steps of:

creating a sixth dielectric layer over the surface of the substrate to form a gate oxide;

depositing a gate material over the sixth dielectric layer; and

patterning the sixth dielectric layer and the gate material to define gate regions of the first and second low conductivity transistors and a gate region of the first conductivity high-voltage transistor.

12. A method of creating an integrated circuit having a second conductivity type low-voltage transistor in a first region, a first conductivity type high-voltage transistor in a second region, and a first conductivity low-voltage transistor in a third region, comprising the steps of:

doping the first and second regions with a first dopant concentration to both control the threshold voltage of the second conductivity type low-voltage transistor and set a breakdown voltage of the first conductivity high-voltage transistor; and

doping the third region with a second dopant concentration to control the threshold voltage of the first conductivity type low-voltage transistor;

wherein an additional voltage threshold adjust implant step to adjust the threshold voltages of the first and second low-voltage transistors is not performed.

14. A method of processing an integrated circuit having a second conductivity type low-voltage transistor in a first region, a first conductivity high-voltage transistor in a second region, and a first conductivity low-voltage type transistor in a third region, comprising the steps of:

doping the first and second regions with a first dopant concentration thereby determining a threshold voltage of the second conductivity type low-voltage transistor and a breakdown voltage of the first conductivity type high-voltage transistor; and

doping the third region with a second dopant concentration; and

excluding the step of:

implanting an additional threshold voltage adjustment of the first and second low-voltage transistors; and

wherein the first and second regions have the substantially the same dopant concentration after processing of the integrated circuit.

16. A method of creating a substrate having multiple regions for creating low-voltage transistors of a first and second conductivity and high-voltage transistors of a first conductivity, comprising the steps of:

creating a defined deposition of a first dielectric layer to expose a first region and a second region; then

implanting a first conductivity dopant into the first and second regions; then

applying a first protective coating over the first and second regions; then

driving in the first conductivity dopant into the substrate; then

removing the first dielectric layer; then

creating a defined deposition of a second dielectric layer in the same location as the defined deposition of the first dielectric layer; then

implanting a second conductivity dopant in the substrate disposed under the defined deposition of the second dielectric layer; then

driving in the second conductivity dopant into the substrate; then

removing the first protective coating and the second dielectric layer; then

creating a patterned third dielectric layer over the surface of the substrate to expose the drain and source of the first and second conductivity low-voltage transistors and the first conductivity high-voltage transistor; then

creating a defined deposition of a fourth dielectric layer disposed on the drain and source of the first conductivity low-voltage transistor; then

applying a second protective coating over the first and second regions; then

implanting a second conductivity dopant into the substrate disposed under the drain and source of the first conductivity low-voltage transistor; then

removing the second protective coating; then

creating a fifth dielectric layer in areas of the substrate where the third dielectric layer is not located; then

removing the patterned third dielectric layer;

creating a sixth dielectric layer over the surface of the substrate to form a gate oxide;

depositing a gate material over the sixth dielectric layer; and

patterning the sixth dielectric layer and the gate material to define gate regions of the first and second low conductivity transistors and a gate region of the first conductivity high-voltage transistor.